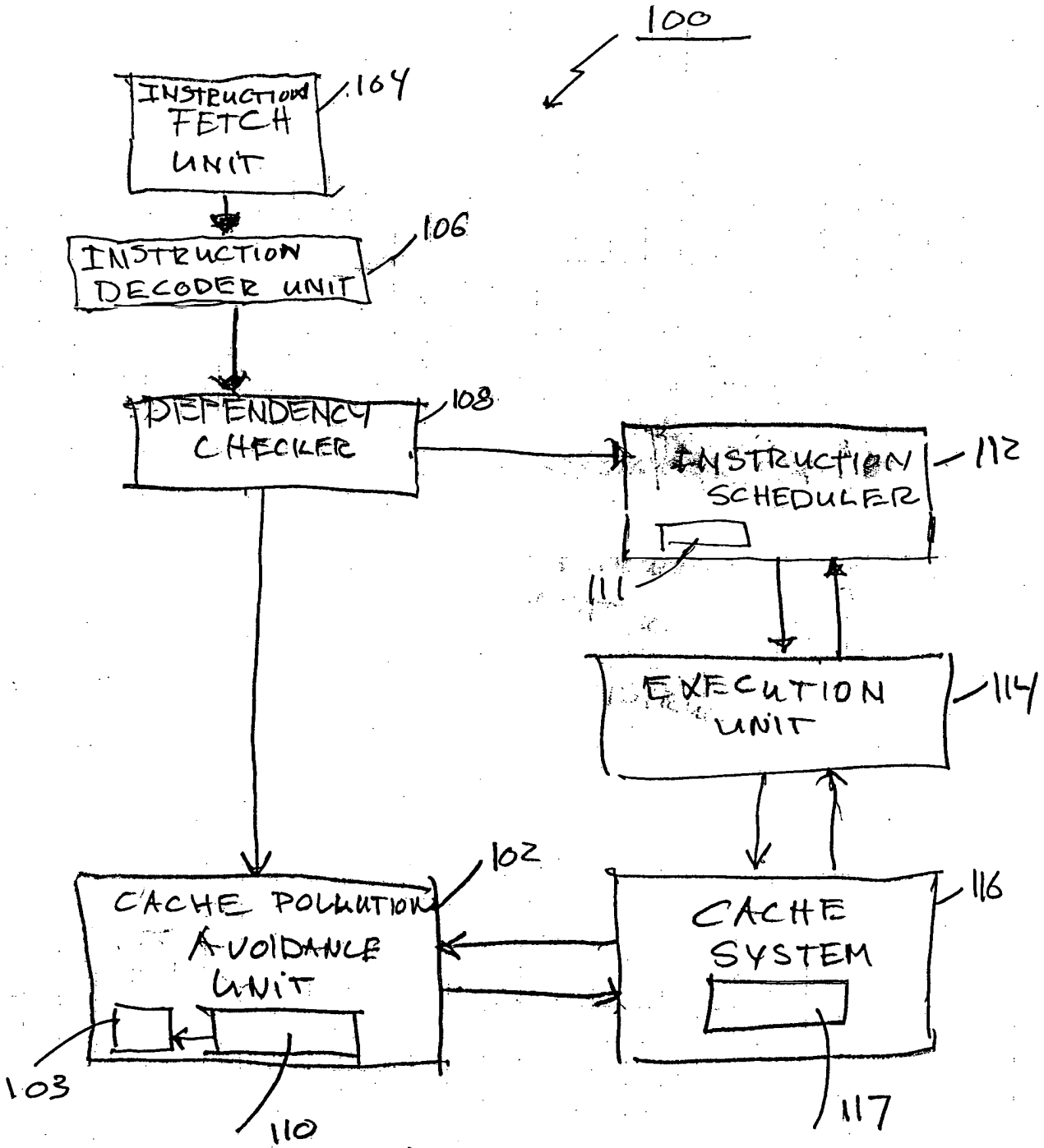

100
INSTRUCTION FETCH UNIT
104
INSTRUCTION DECODER UNIT
106
DEPENDENCY CHECKER
108
INSTRUCTION SCHEDULER
112
111
EXECUTION UNIT
114
CACHE POLLUTION AVOIDANCE UNIT
102
CACHE SYSTEM
116
103
110
117

FIG. 1

200

Instruction	Type	Operation
A	Producer Load	LOAD (address1, r1)
B	Calculation	ADD (r1,r2,r3)
C	Consumer Load	LOAD (address2=r3, r4)
D	Independent Load	LOAD (address3=r5, r6)

FIG. 2

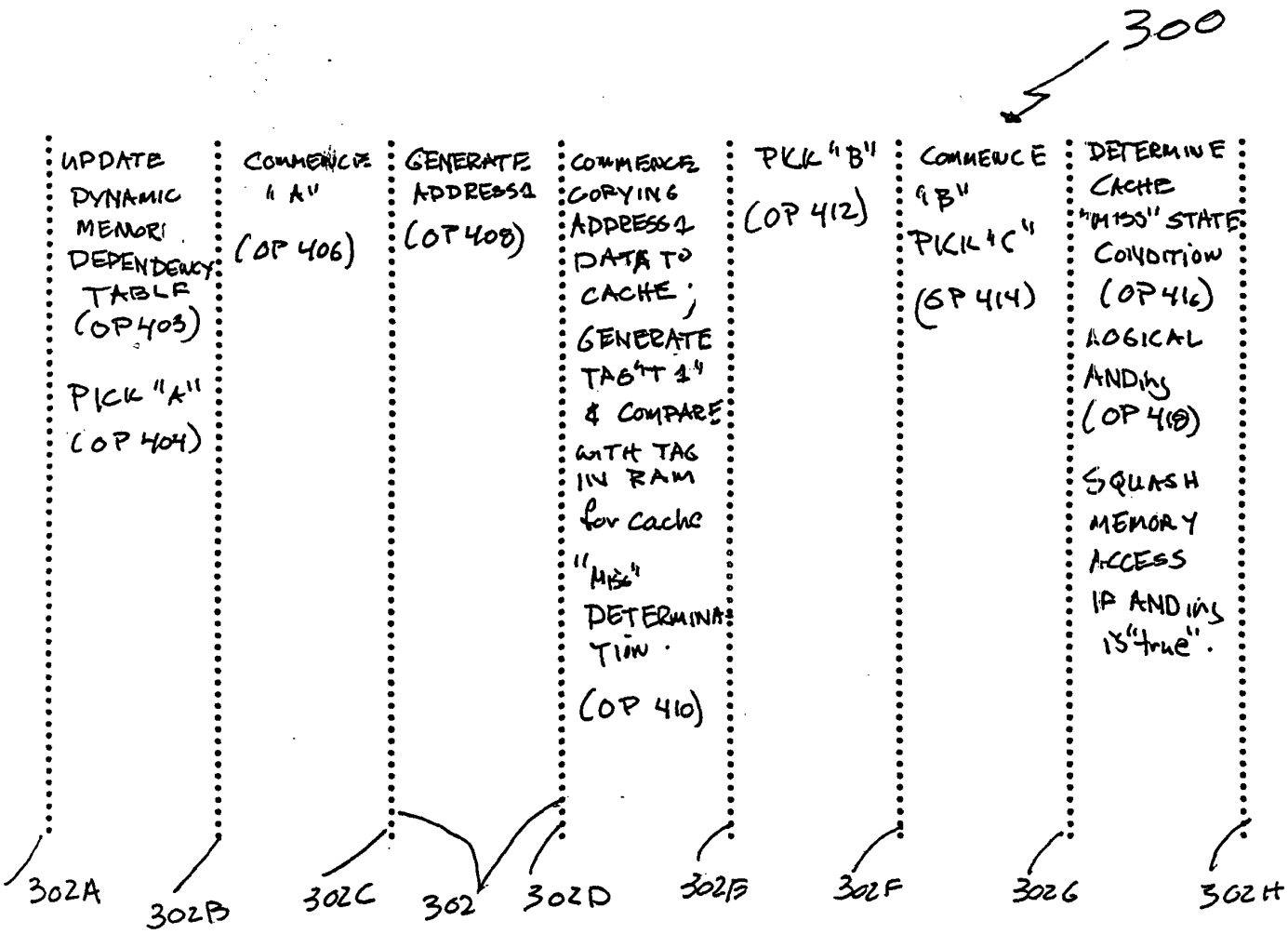

300
UPDATE DYNAMIC MEMORY DEPENDENCY TABLE (OP 403)
PICK "A" (OP 404)
COMMENCE "A" (OP 406)
GENERATE ADDRESS 1 (OP 408)
COMMENCE COPYING ADDRESS 1 DATA TO CACHE; GENERATE TAG "T 1" & COMPARE WITH TAG IN RAM for cache "MISS" DETERMINATION. (OP 410)
PICK "B" (OP 412)
COMMENCE "B" PICK "C" (OP 414)
DETERMINE CACHE "MISS" STATE CONDITION (OP 416)
LOGICAL ANDing (OP 418)
SQUASH MEMORY ACCESS IF ANDing IS "true".
302A
302B
302C
302
302D
302E
302F
302G
302H

FIG. 3

400

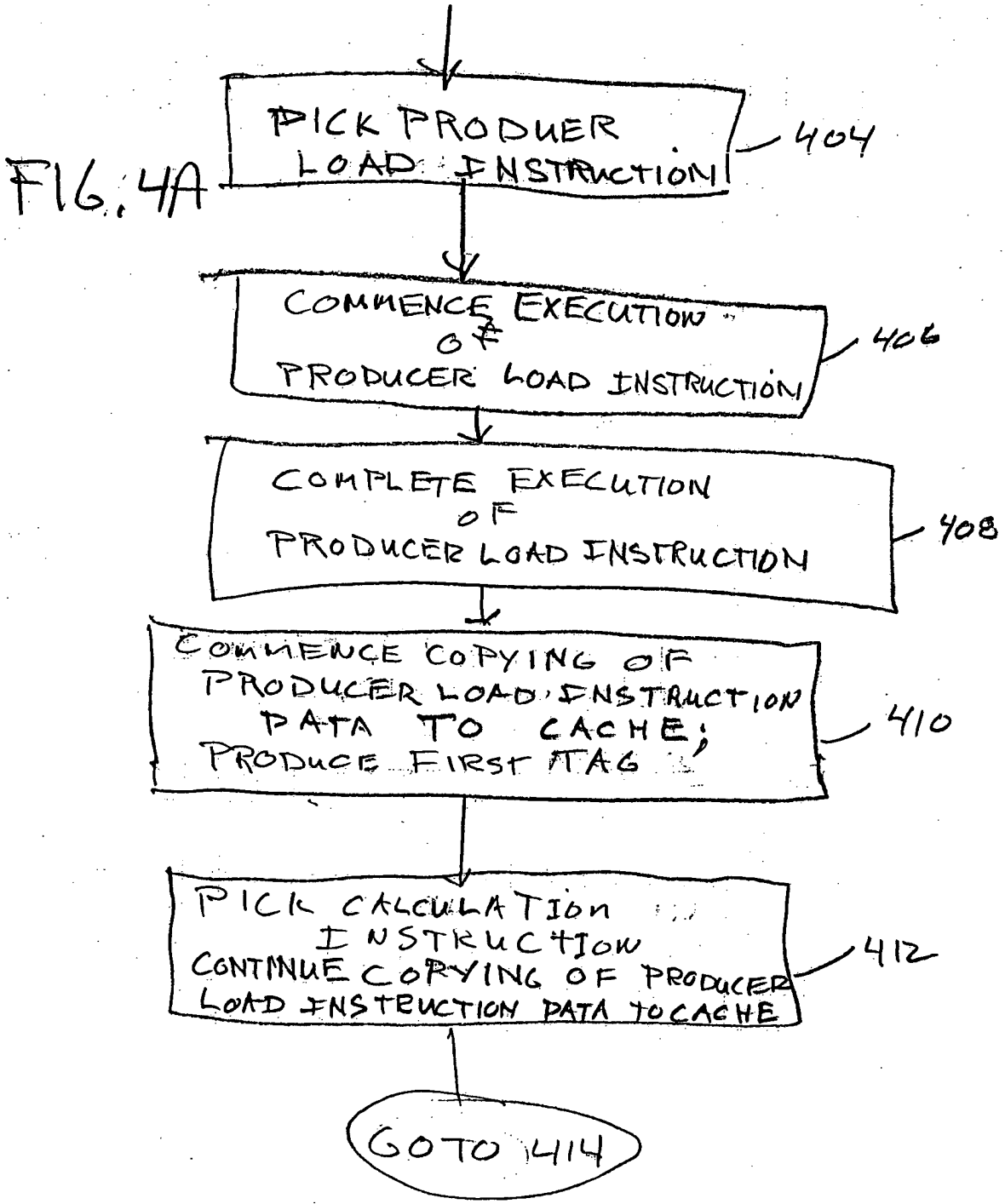

PICK PRODUER LOAD INSTRUCTION
404
COMMENCE EXECUTION OF PRODUCER LOAD INSTRUCTION
406
COMPLETE EXECUTION OF PRODUCER LOAD INSTRUCTION
408
COMMENCE COPYING OF PRODUCER LOAD INSTRUCTION DATA TO CACHE; PRODUCE FIRST TAG
410
PICK CALCULATION INSTRUCTION CONTINUE COPYING OF PRODUCER LOAD INSTRUCTION DATA TO CACHE
412
GOTO 414

FIG. 4A

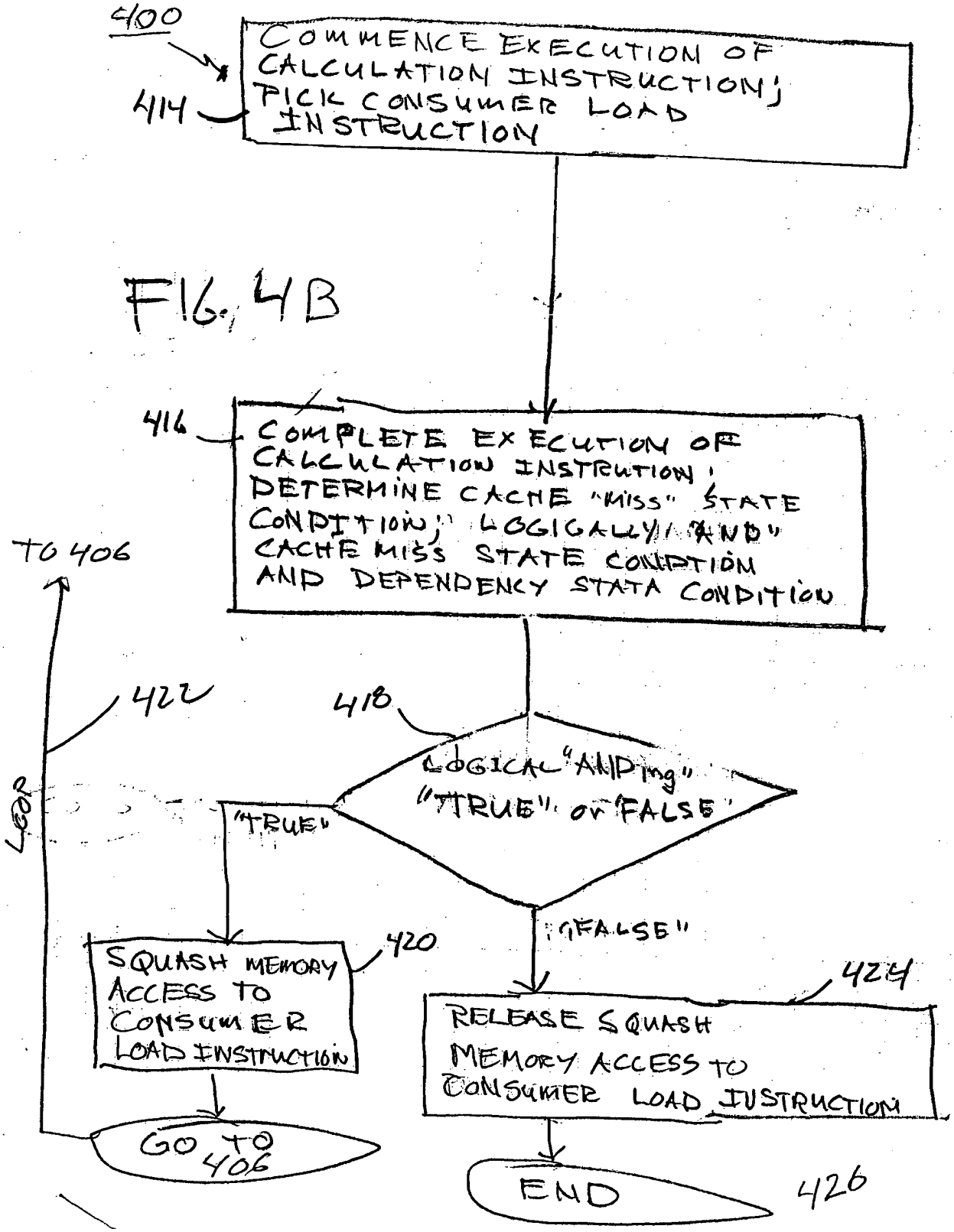
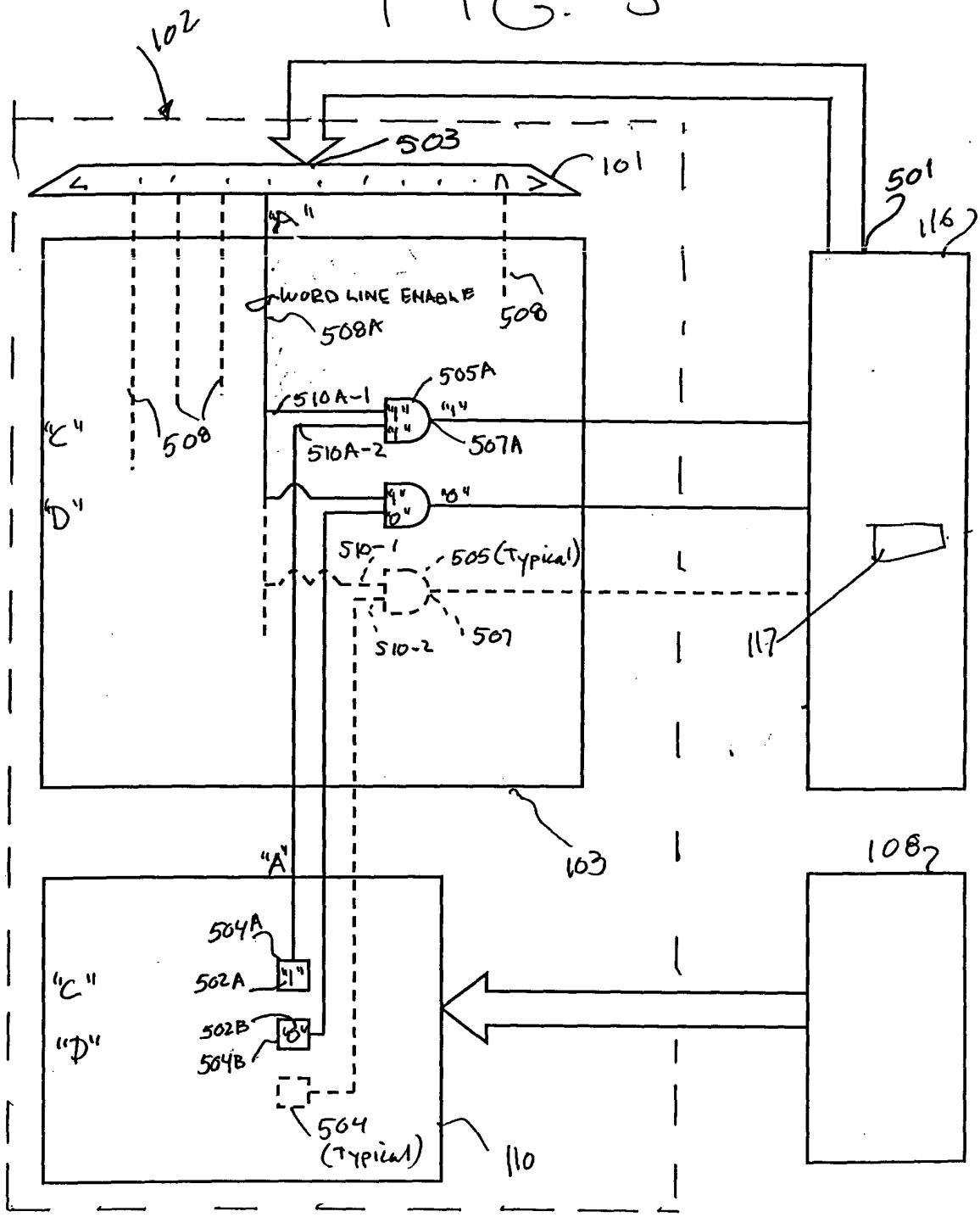

400
COMMENCE EXECUTION OF CALCULATION INSTRUCTION; PICK CONSUMER LOAD INSTRUCTION
414
416
COMPLETE EXECUTION OF CALCULATION INSTRUCTION; DETERMINE CACHE "MISS" STATE CONDITION; LOGICALLY "AND" CACHE MISS STATE CONDITION AND DEPENDENCY STATE CONDITION
418
LOGICAL "ANDing" "TRUE" or "FALSE"
"TRUE"
"FALSE"
420
SQUASH MEMORY ACCESS TO CONSUMER LOAD INSTRUCTION
422
LOOP
TO 406
GO TO 406
424
RELEASE SQUASH MEMORY ACCESS TO CONSUMER LOAD INSTRUCTION
END
426

FIG. 4B

FIG. 5


102
503
101
501
116
"B"
WORD LINE ENABLE
508A
508
505A
510A-1
"1"
"C"
508
510A-2
507A
"0"
"D"
510-1
505 (Typical)
510-2
507
117
103
108
"A"
504A
"C"
502A
"1"
502B
"0"
"D"
504B
504
(Typical)
110